AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 6, with the following rewritten paragraph:

--On the other hand, when the yield rate of the acceptable semi-finished semiconductor devices is larger than the predetermined permissible rate, the silicon wafer concerned is subjected to a customization process in which the custom-purpose wiring-arrangement section of the multi-layered wiring-arrangement of each semi-finished semiconductor device is rearranged in accordance with a customer's request. Namely, the customization is ~~curried~~ carried out by locally cutting the circuit pattern formed in the uppermost metal circuit pattern layer of the custom-purpose wiring-arrangement section, using a photolithography method and an etching method, such that the uppermost circuit pattern concerned is rearranged in accordance with the customer's request, resulting in production of the finished semiconductor devices on the silicon wafer.

Please replace the paragraph beginning at page 14, line 13, with the following rewritten paragraph:

--Of course, although the serial chip-numbers [001] to [156] are conveniently and representatively shown in Fig. 1, in reality, these serial chip-numbers [001] to [156] are not written in the chip areas 12. As shown in Fig. 1, the silicon wafer

[[20]] 10 features an orientation flat 15 formed by cutting a part thereof, and the numbering of the chip areas 12 is carried out with respect to the orientation flat [[14]] 15. Namely, it is possible to recognize a chip-number of each chip area 12 based on a relative position of the chip area 12 concerned in relation to the orientation flat [[14]] 15.--